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DESIGN OF PFC CONVERTER BASED ON INTERLEAVE BOOST

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ПРОЕКТ ПРЕОБРАЗОВАТЕЛЯ КОРРЕКЦИИ КОЭФФИЦИЕНТА МОЩНОСТИ НА ОСНОВЕ ЧЕРЕДОВАНИЯ УСИЛЕНИЯ

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Abstract. Based on the principle of stagger boost PFC, this paper expounds the application value of stagger PFC theory by developing a scientific and feasible scheme and using Matlab simulation. According to the subject requirements, the use of UCC28070 to achieve PFC control function. And learn IC functions. Based on the theory of interlaced PFC, the most suitable electronic device is selected to adjust each part of the circuit. Finally, Solidworks and Protel software were used to draw the radiator and PCB boards, then the prototype was made and debugged, and the final result was obtained.

Аннотация. Приводится прикладное значение теории ступенчатой коррекции коэффициента мощности путем моделирования в Matlab в соответствии с требованиями субъекта. На основе теории чередующейся коррекции коэффициента мощности выбрано наиболее подходящее электронное устройство для настройки каждой части схемы. В программах Solidworks и Protel были выполнены радиатор и платы печатных плат, затем изготовлен и отлажен прототип и получен окончательный результат.

Keywords: boost circuit, PFC technology, energy conservation, environmental conservation, efficiency.

Ключевые слова: цепь усиления, технология коррекции коэффициента мощности, экономия энергии, охрана окружающей среды, эффективность функционирования.

Due to the rapid development of PFC technology, power factor correction PFC pre-regulators have been widely used in primary industrial switching power supplies and household electricity. The traditional single-weight PFC solution is no longer applicable to today's single-phase active

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PFC technology, power electronic devices, and power levels that are constantly improving. Due to the increasing power demand, the voltage and current pressure requirements for a single PFC switching device to resist are getting higher and higher, and there are a lot of difficulties in selecting devices, and the current and voltage at some key points of the circuit change very large instantaneously, resulting in conducted EMI and radiated [1].

The interleaved PFC technology has been put into use in recent years, and the interleaved PFC technology actually refers to the power factor correction PFC technology. The application of this technology has brought many benefits, such as reducing the input current ripple and reducing the withstand voltage and current requirements of power devices; the capacity of a single inductor is reduced, and the output power is increased, thereby greatly reducing the entire power circuit [2].

This design is based on the design and development of the power factor correction part of the on-board charging power supply for electric drive vehicles. The main goal is the primary PFC pre-regulation circuit of the on-board power supply. The interference of the electric vehicle power supply increases the power factor, reduces the amount of harmonics, and makes it more environmentally friendly and green [3].

Parameter Design of Main Circuit Components

Based on the characteristics of the chip and the requirements of the experimental circuit, the parameters of each component of the boost circuit of the main unit can be obtained with the help of relevant formulas. The implementation process is as follows. Based on the chip application manual, the ratio of the input ripple current to the ripple current of a single inductor can be obtained. In the two-phase interactive PFC, it is a function of the duty cycle, because the inductor ripple can be offset by a certain method, so there is no need to worry about a single inductor even if there is a large ripple. Usually, the determination of the boost inductor mainly depends on the maximum ripple current. In the full-cycle input state, the maximum ripple can be determined at the peak of the bottom line voltage. Based on the chip manual, the specific value of the inductance at full load can be obtained [4].

$$D = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390 - 180\sqrt{2}}{390} \approx 0.35$$

$$K(D) = \frac{1 - 2 \times D}{1 - D} = \frac{1 - 2 \times 0.35}{1 - 0.35} = 0.462$$

$$\Delta I_L = \frac{P_{OUT} \times \sqrt{2} \times 0.3}{V_{IN\_MIN} \times \eta \times K(D)} = \frac{3600 \times \sqrt{2} \times 0.3}{180 \times 0.9 \times 0.462} \approx 19.96\text{A}$$

$$L_{MIN} = \frac{V_{IN\_MIN}\sqrt{2} \times D}{\Delta I_L \times f_S} = \frac{180\sqrt{2} \times 0.69}{19.96 \times 100k} \approx 45\mu\text{H}$$

Under light load conditions, the maximum possible inductance is:

$$L_{MAX} = 255\mu\text{H}$$

Finally choose the average value as the inductance value:

$$L_{avg} = \frac{L_{MIN} + L_{MAX}}{2} = 150\mu\text{H}$$

Average maximum current through a single inductor:

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$$I_{Lav} = \frac{P_{OUT}}{2 \times \eta \times V_{MIN}} = \frac{3600}{2 \times 0.9 \times 180} = 11.1A$$

From the above calculations, it can be seen that the final selected single inductance value can withstand a limit current of 11.1A. In order to ensure that the system has good scalability and safety, the actual current withstands value is designed to be 20A. In addition, because it is high-frequency work, so A ferrite core is chosen [5].

Usually, the determination of the output capacitor mainly depends on the actual demand for filtering power frequency ripple:

$$C_{OUT} = \frac{\frac{2 \times P_{OUT}}{f_{LINE}}}{V_{OUT}{}^2 - (0.75 \times V_{OUT})^2} = \frac{\frac{2 \times 3600}{47}}{390^2 - (292.5)^2} \approx 2700\mu H$$

For this capacitance, the voltage ripple at the output peak V_{RIPPLE} It can be obtained by the following formula:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{2\pi \times \eta \times V_{OUT} \times 2 f_{LINE} \times C_{OUT}} \approx 12.9V$$

Through the above calculation, we can know that three 1000 uF capacitors that can withstand 450V voltage are finally selected to be connected in parallel.

Selection of power switch tube and output diode. The determination of output diodes and power switch tubes mainly depends on indicators such as peak current, average current, and operating voltage. As far as peak current is concerned, it can be obtained with the help of the following formula, namely:

$$I_{PEAK} = (\frac{\sqrt{2} P_{OUT}}{2 \times V_{IN\_MIN} \times \eta} + \frac{\Delta I_L}{2}) 1.2 \approx 30.9A$$

As for the average current of the switch tube and the output diode, it can be obtained by using the following formula in turn, namely:

$$I_{DS} = \frac{\frac{P_{OUT}}{\eta}}{2\sqrt{2} \times V_{IN\_MIN}} \sqrt{2 - \frac{16\sqrt{2} V_{IN\_MIN}}{3\pi \times V_{OUT}}} \approx 7.42A$$

$$I_D = \frac{P_{OUT}}{V_{OUT}} = \frac{3600}{2 \times 390} \approx 4.62A$$

Through the above calculation, it can be seen that the voltage that the diode and the switch tube need to withstand is 400V. Based on this, it is finally determined that the switch tube is selected as FDH44N50, and the diode is selected as DES12x31-06C.

PFC control circuit design. Clock Setting and Maximum Duty Cycle Clamping [6].

The role of the resistors R_{RT} R_{DMX} is to set the operating frequency of the chip and the maximum output duty cycle, which can usually be obtained in sequence with the help of the following formulas:

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$$R_{RT}=\frac{7.5\times10^{9}\,\Omega}{f_S}=\frac{7.5\times10^{9}\,\Omega}{100k}=75\text{k}\Omega$$

In order to effectively protect the switching tube, the maximum duty cycle generally does not exceed 0.97, $R_{\text{DMX}}=R_{RT}(2\times D_{MAX}-1)=68.1\text{k}\Omega$.

1. Front-end and back-end sampling network

R_A、R_B meaning of the representative is the front and rear end voltage divider network used for voltage sampling. In order to control the input current of VSENSE and VINAC as much as possible and reduce the power consumption of PFC, generally choose a larger resistance R_A， in series in the system circuit， $R_A=3.2M\Omega$， R_B The output voltage can be effectively adjusted:

$$R_B=\frac{\frac{V_{REF}}{2}\times R_A}{V_{OUT}-\frac{V_{REF}}{2}}=\frac{3\times3.2M}{390-3}\approx24.9k\Omega$$

In order to effectively protect the circuit system, it is necessary to set the threshold voltage of the overvoltage protection OVP:

$$V_{OVP}=3.18\frac{R_A+R_B}{R_B}=3.18\frac{3.2M+24.9k}{24.9k}\approx412V$$

In order to reduce or even eliminate the influence of high-frequency clutter on the sampling signal, it is usually necessary to R_B A small capacitor is connected in parallel for filtering processing. Based on the actual working environment and the frequency response of the capacitor, the setting is 220pF.

The design method of voltage loop compensation is usually constructed on the basis of the compensation method designed by Llgd-Dixon. In this research, the design will be based on the chip manual [7]. The main function is to offset the low-frequency ripple, and try to ensure that the low-frequency ripple is controlled at 3% of the output voltage, so as to achieve higher transmission efficiency and reduce the current distortion rate. Regarding the gain of the voltage amplifier and the voltage divider network, the following formula can be used to calculate:

$$gm_v=70\mu s$$

$$H=\frac{V_{VREF}}{V_{OUT}}=\frac{3}{390}\approx0.0077$$

In terms of output impedance Z_O, its main role is to offset the output ripple， V_{ripple}. The main role is to control its effective output voltage ratio of 20% (ΔV_{AO}) Impact. And about the feedback capacitor C_{PV} can be determined by the following formula.

$$\Delta V_{AO}=3.2\text{V}$$

$$Z_O=\frac{\Delta V_{AO}\times0.03}{V_{ripple}Hgms}=\frac{3.2\times0.03}{12.9\times0.0077\times70\mu}=13.8\text{k}\Omega$$

$$C_{PV}=\frac{1}{2\pi\times2f_{LINE}Z_O}=\frac{1}{2\pi\times2\times47\times13.8k}\approx124\text{nF}$$

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Further, the crossover frequency of the voltage loop can be obtained f_{cv},

$$f_{cv}=\sqrt{H\times gms\times\frac{P_{OUT}}{\eta\times\Delta V_{AO}\times j4\pi^2\times C_{OUT}\times V_{OUT}\times C_{PV}}}\approx 33.26\text{Hz}$$

Voltage loop compensation resistor R_{ZV} Usually placed at the frequency across which the voltage loop compensates for the capacitor C_{ZV} The main function of is to increase the gain of the voltage loop, and the two can usually be obtained by the following formula:

$$R_{ZV}=\frac{1}{2\pi\times f_{cv}C_{PV}}\approx 33\text{k}\Omega$$

$$C_{ZV}=\frac{1}{2\pi\times\frac{f_{CV}}{10}\times R_{ZV}}\approx 1.5\mu\text{F}$$

Connect the PKLMT pin externally to R_{PK1} as well as R_{PK2}, It can effectively adjust the current limit comparator inside the system. Based on the chip manual, this design is set to 4V. R_{PK1} The default is 3.65k, then $R_{PK2}=\frac{V_S\times R_{PK1}}{V_{REF}-V_S}=\frac{4\times 3.65k}{6-4}\approx 7.5\text{k}\Omega$

At present, there are mainly three kinds of current transformers commonly used in experiments, namely: CS4050V-01L, CS4100V-01L and CS4200V-01L. The principle mainly depends on the primary current frequency. Based on the selection manual, the CS4200V-01L transformer was finally determined.Transformer sense resistor R_S. The determination usually depends on the reference voltage V_S, In this design, the reference voltage is set to 4V, and a 10% margin is left here, and then the R_S, $R_S=\frac{0.9\times V_S\times N_{CT}}{I_{PEAK}}=\frac{0.9\times 4\times 200}{30.9}\approx 23.7\Omega$.

In addition, to ensure that the transformer achieves volt-second integration at the highest duty cycle, it is usually necessary to construct a reset network, resistor R_R The main function of is to ensure the reset of the transformer, which can be obtained based on the following formula:

$$R_R\geq\frac{R_S\times D_{MAX}}{1-D_{MAX}}=\frac{23.7\times 0.97}{1-0.97}\approx 750\Omega$$

Because the UCC28070 realizes the synthesis of the inductor current by collecting the current of the switch tube, usually a resistor is connected to its RSYNTH terminal R_{syn} It is used to set the current, which can be obtained with the help of the following formula:

$$R_{SYN}=\frac{200\times 255\mu\times\frac{24.9}{24.9+3200}}{23.7}\approx 180\text{k}\Omega$$

Connect the output of the multiplier to a resistor R_{IMO}, It is used to reasonably set the linear region of the multiplier, which can usually be obtained with the help of the following formula:

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$$IMO = \frac{17\times10^{-6}\times V_{INAC}(V_{VAOMAX}-1)}{K_{vff}} = \frac{17\times10^{-6}\times1.5\times(5-1)}{1.156} = 88\mu A$$

$$P_{in(\max)} = \frac{1.1\times P_{out}}{\eta} = \frac{1.1\times3600}{0.92} = 4304W$$

$$I_{in(pk)} = 2\times\frac{P_{in(\max)}}{V_{in}} = 2\times\frac{4304}{180} = 47.8A$$

$$R_{IMO} = \frac{0.5\times I_{in(pk)}\times R_S}{N_{CT}\times I_{IMO}} = 45k\Omega$$

Regarding the switching frequency of the PFC current loop, the general range is between 1/10-1/6. In this design, by combining the actual needs and the working environment, the final choice is 1/10, in order to effectively compensate the current loop, need to know the power stage gain Gps of the current loop, select Rzc, Czc, Cpc as follows:

$$G_{PSC} = \frac{V_{OUT}\times R_S\times\frac{1}{N_{CT}}}{2\pi\times\frac{f_S}{10}\times L_{AVG}\times V_{RAMP}} = \frac{390\times23.7\times\frac{1}{200}}{2\pi\times\frac{100k}{10}\times150\mu\times4} \approx 1.2$$

gm_C is the trans conductance current amplifier gain:

$$gm_C = 100\mu s$$

$$R_{ZC} = \frac{1}{gm_C\times G_{PSC}} \approx 9.1k\Omega$$

$$C_{ZC} = \frac{1}{2\pi\frac{f_S}{10}\times R_{ZC}} \approx 2.2nF$$

$$C_{PC} = \frac{1}{2\pi\frac{f_S}{2}\times R_{ZC}} \approx 330pF$$

Soft start and frequency dithering mode setting

1. Soft start. Usually a capacitor is connected to the SS pin C_{SS}, for soft start time t_{SS} In this design, by combining the actual needs and the working environment, the final choice is 0.2s. Regarding the determination of the capacitance, the calculation formula is as follows:

$$C_{SS} = \frac{10\mu A\times0.2s}{2.25V} \approx 1\mu F$$

2. Frequency jitter setting (reduce EMI). Based on the chip manual, it can be learned that the variable frequency mode can effectively reduce EMI。. External R_{RDM} and C_{CDR} Used to set frequency jitter amplitude and rate. For this design, use the default dither settings:

$$f_{DM} = 30kHz \quad , \quad f_{DR} = 10kHz$$

The corresponding resistor and capacitor settings are: $R_{RDM} = 31.6k\Omega$ $C_{CDR} = 220pF$.

Regarding the driver of Mosfet, MIC4422 IC is used, which is a low-power driver chip, of which 1 is the power supply pin (VS), 2 is the input pin (IN), 3 is the empty pin (NC), 4 5 and 5 are

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ground pins (GND), and pins 6 and 7 are output pins (OUT) (Figure 1).

The power supply is 12V, and the purpose of connecting an external 1uF capacitor is to stabilize the voltage. In addition, a 0.1uF bypass decoupling capacitor is added to eliminate voltage glitches. Based on the principle of reducing switching loss, the steeper the front and rear edges of the driving waveform, the better, and the driving source is provided by a stable voltage [8]. However, as far as conventional switching devices are concerned, wiring inductance is very likely to occur, causing failure of the drive, which will affect the stability and safety of the circuit system. In order to properly solve the above problems, it is usually necessary to connect a resistor in series with the gate of the MOSFET to ensure that the oscillation damping is within the specified range. However, the addition of resistance creates a new problem, that is, it may affect the voltage characteristics of the drive to a certain extent, reducing the drive current, making the front and rear edges steeper, and significantly increasing the loss [9]. Therefore, the added gate resistance should not be too large as much as possible, just to reduce the oscillation. Combined with the actual situation, the driving resistance of 3.3 is selected here. Because there is a junction capacitance between the gate and source of the MOSFET, the junction capacitance will be charged as long as the system is powered on. In order to avoid damage to the MOSFET due to excessive junction capacitance, a discharge resistor needs to be connected in parallel between the gate and source. According to engineering experience, select a value of 10k. Relay protection circuit in order to ensure the reliability, safety and efficiency of the circuit, the primary circuit is usually controlled by means of a relay. The general circuit diagram is shown in Figure 2 below.

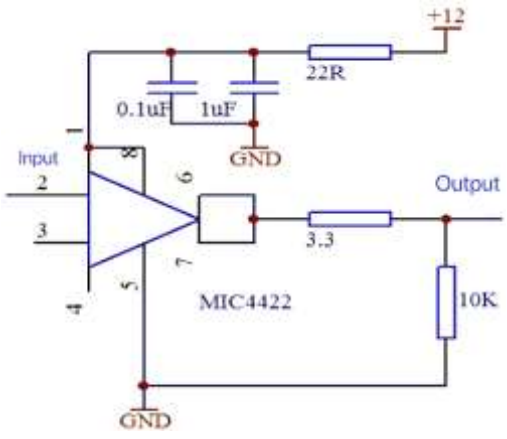

Figure 1. MIC4422 drive circuit

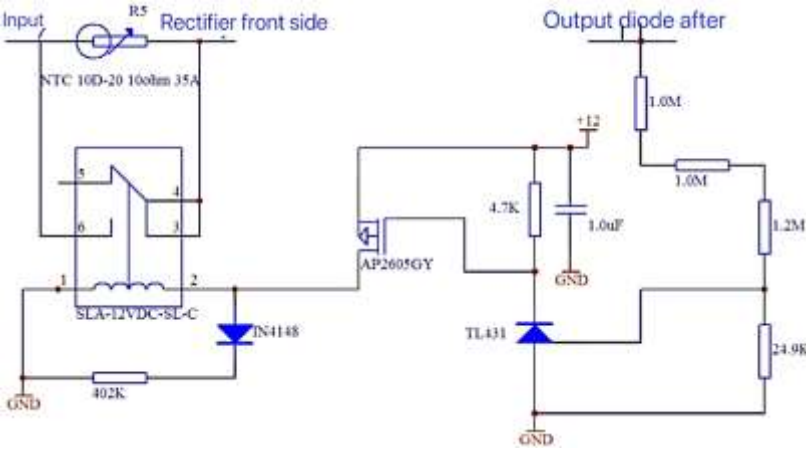

Figure 2. The working principle and process are introduced as follows

1. TL431 is a shunt regulator integrated circuit. It is mainly composed of the following parts: output switch tube, voltage comparator and 2.5V reference voltage source, etc. If the input voltage is lower than 2.5V, the system will be in the disconnected state. When the input voltage is equal to or exceeds 2.5V, the system will operate normally. Here use TL431 to form the relay control circuit.

2. As shown in Figure 2, before the UCC28070 is officially running, the system will use a negative temperature coefficient resistor to control the current. If the output of the main circuit is 324V, the voltage divider network will be assigned a 2.5V comparison voltage input to the TL431, which will immediately start the working mode, and a P-channel enhanced MOSFET is connected to the output terminal. The power supply is 12V. At this time, the MOSFET is turned on. Based on the above figure, it can be known that the relay pulls in, which will change the current flow direction at the input side of the main circuit, thereby reducing system loss.

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3. When the output voltage drops, the TL431 will be interrupted, the MOSFET will also stop working, and the relay will also be disconnected. At this time, under the action of the inductive effect, the relay coil will generate current, so a discharge circuit is required, otherwise it will be damaged system. The solution is to form a discharge circuit on the relay coil with the help of diodes and resistors [10].

As far as the auxiliary power supply is concerned, its main function is to provide a +12V power supply for relays and MOSFETs. The general circuit diagram is shown in Figure 3-6 below.

Connect a +15V switching power supply to output +12V voltage. When the output voltage is greater than +12V, use resistors to divide the voltage to form a voltage not lower than 2.5V. In this case, TL431 will be connected immediately, and then the voltage of the triode will be lowered, causing the triode to stop running. And then make +15V power supply interruption. And when the output is less than +12V, TL431 will interrupt the operation, the base voltage of the triode will rise to 15V, and then the output will increase. The above is a simple triode voltage regulator circuit. In order to reduce or even completely offset the electromagnetic interference, it is necessary to design a filter circuit. The approximate circuit diagram is shown in Figure 4 below.

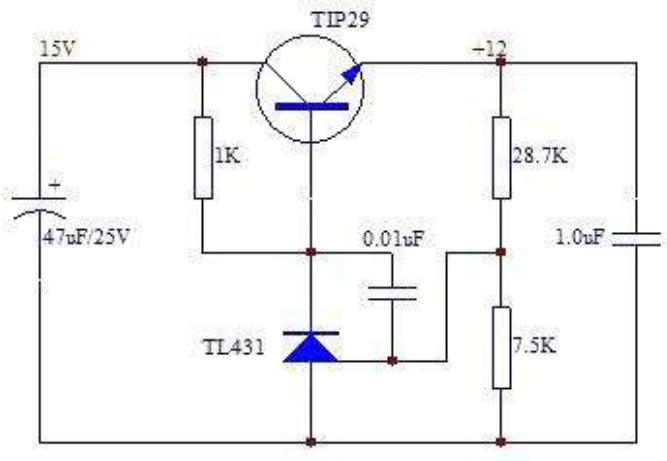

Figure 3. The working principle is as follows

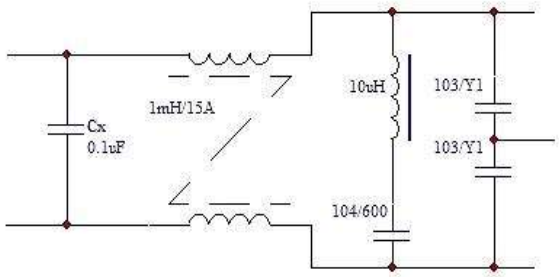

Figure 4. The filter circuit

As far as the filter circuit is concerned, it is mainly composed of the following parts: namely, a resonant filter, a common mode inductor, an x capacitor, and a y capacitor. Based on lookup table selection: C_X=0.1μF ， C_Y=0.01μF ， L=1mH

The determination of the resonant filter is mainly determined by the frequency to be filtered out. In this design, the switching tube is 100k, and then it can be seen that the clutter is also 100k. Take $C = 0.1\mu F$， Then the resonant inductance can be obtained, namely:

$$L = \frac{1}{4\pi^2 f_s^2 C} = 25\mu H$$

In this study, for the PFC of the interleaved boost, the simulation analysis was carried out with the help of matlab software. When performing simulation analysis, the relevant parameters usually need to be known in advance and meet certain requirements. Here the simulation time is 0.5s. AC input Vin=220V,output 400V, switching frequency 100kHz, load resistance 50 (3600W), inductance 150uH, output capacitance 2700uF, these parameters are obtained from the previous analysis and calculation.

Based on the above parameters, the obtained simulation results are shown in Figure 5 below.

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Simulation waveforms of inductor interleaving ripple and output diode ripple. Based on the content in the above figure, it can be known that under the conditions of voltage regulation and unity power factor correction, the interleaved boost PFC can reduce the output ripple by 50%, effectively reducing loss and cost, and reducing EMI Figure 5-8.

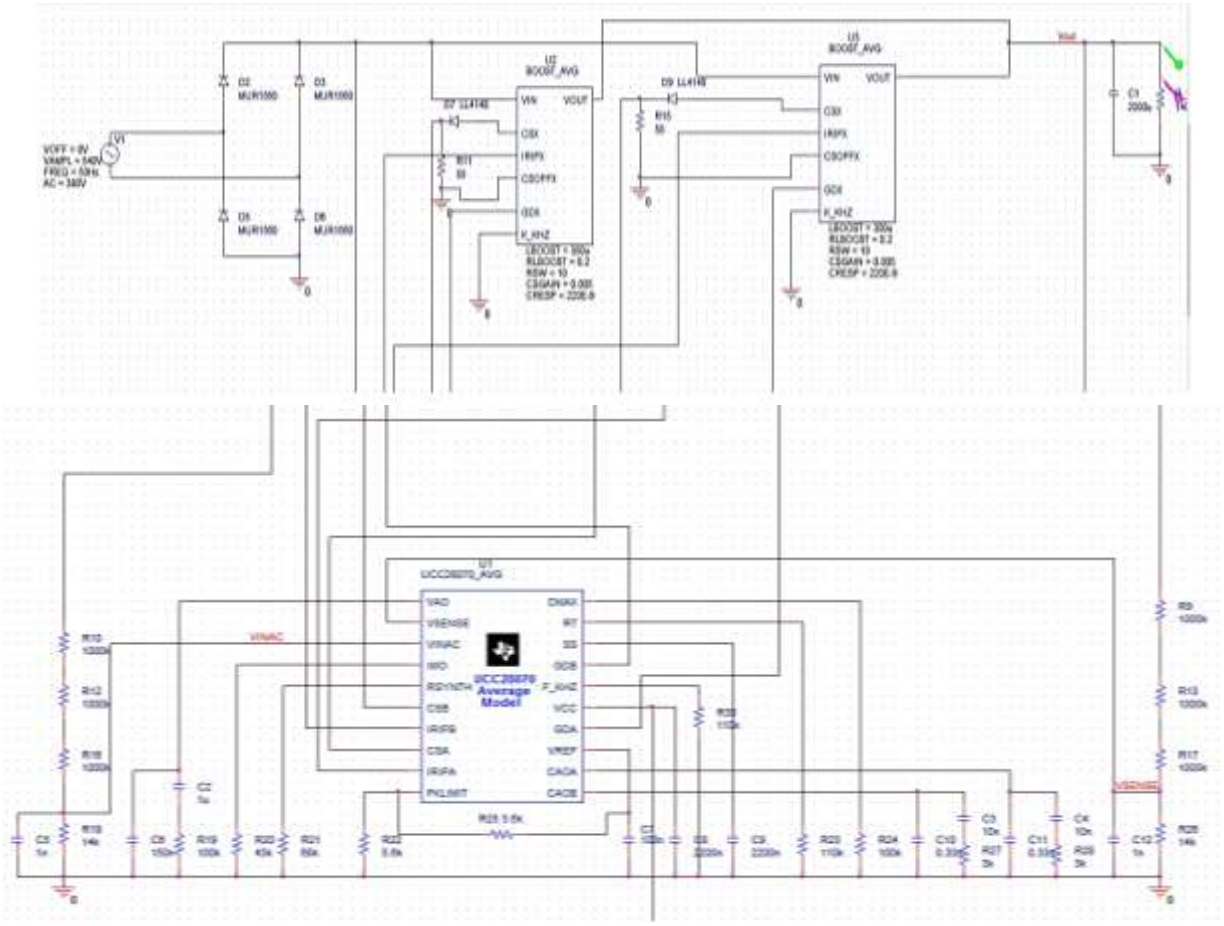

Figure 5. Input and output voltage simulation waveforms

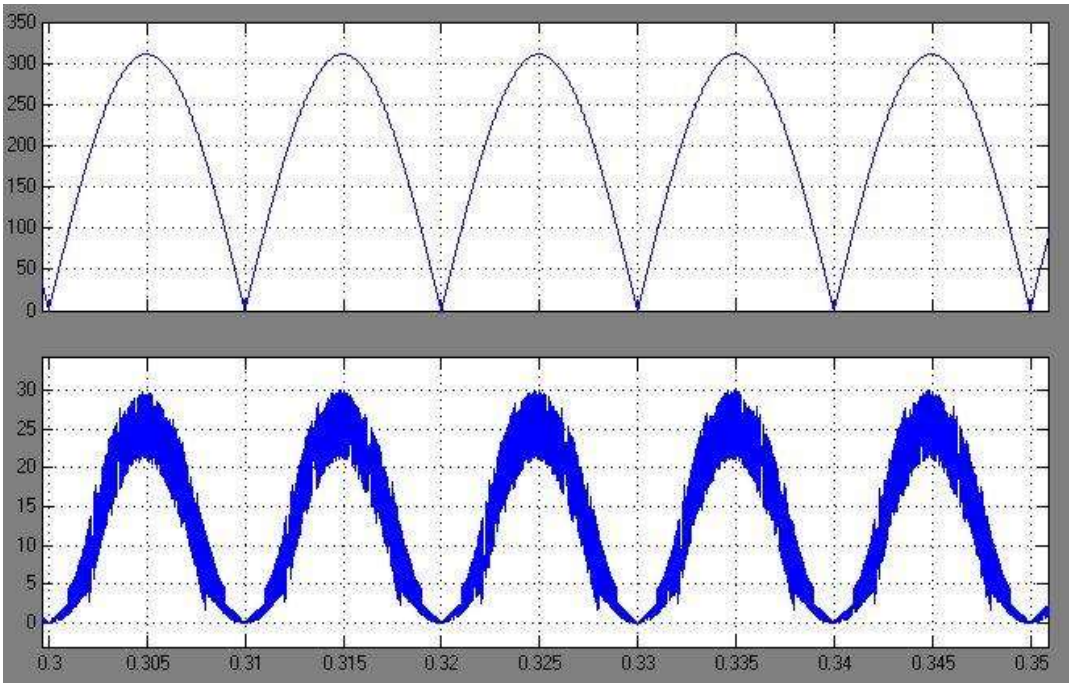

Figure 6. Input voltage and current simulation waveforms on the rear side of the rectifier bridge

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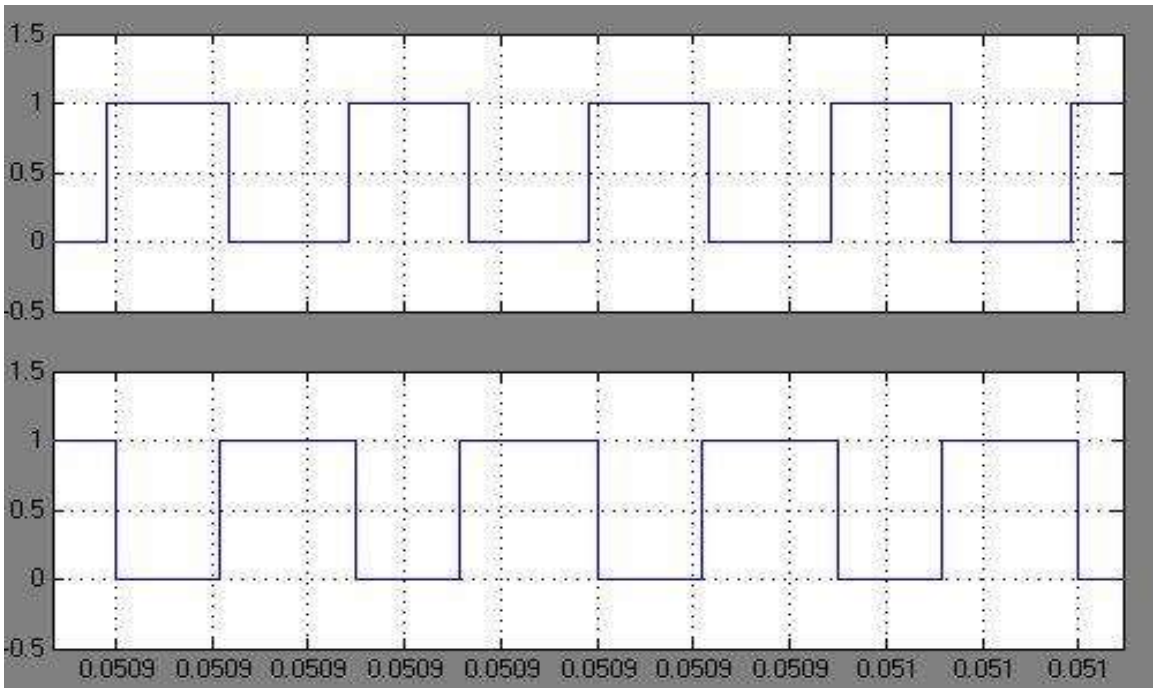

Figure 7. Interleaved 180° pulse waveform

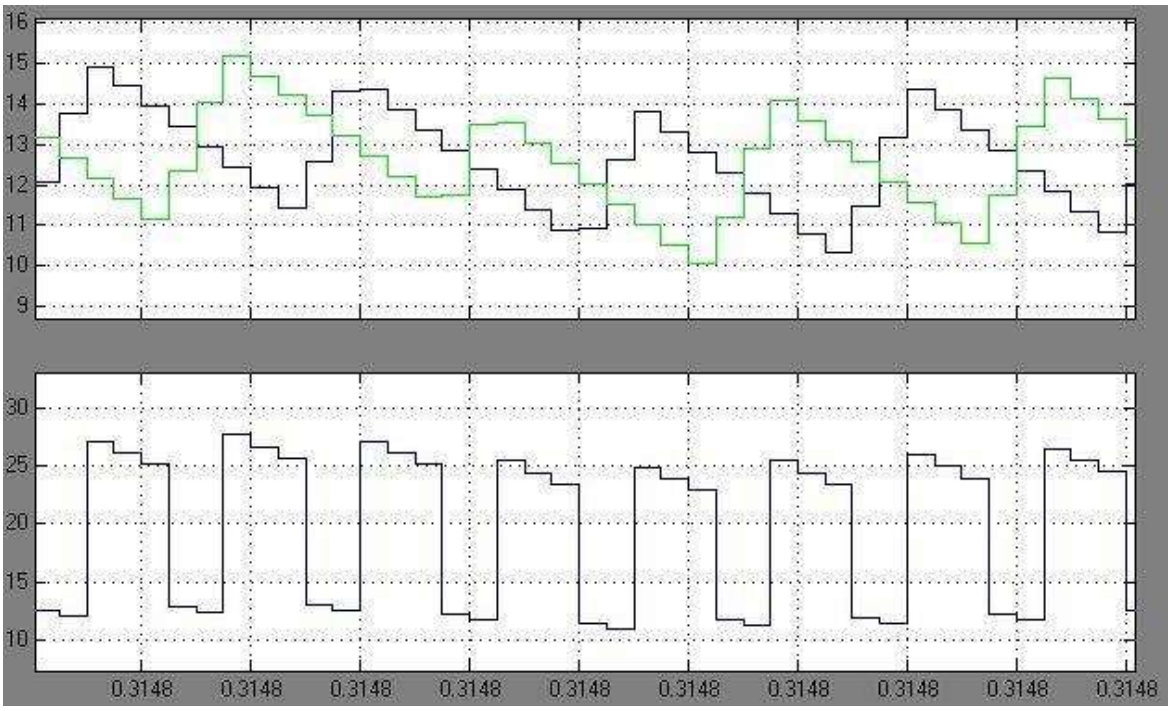

Figure 8. Simulation waveforms

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